

# LAST CALL FOR PAPERS

## 3<sup>rd</sup> International Design and Test Workshop

<http://www.enis.rnu.tn/tttc-idt>



### IDT'08

Monastir-Tunisia  
El Habib Hotel

December 20-22 2008 



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This event provides a unique forum to discuss novel approaches in design, automation and test in the Middle East and Africa (MEA) region for researchers and practitioners in the areas of VLSI design, test and fault tolerance to come together to discuss new research ideas and present new research results. This event will provide the only VLSI Design & Test-specific meeting in the MEA region. Workshop topics include all aspect of design, test and automation. Specific topics are to include:

- System Specification and Modelling
- System Design Methods
- SOC/NOC/MPSOC
- Quantum MEMs
- Architectures and Nanotechnology architectur
- Reconfigurable Computing
- Emerging Technologies, Systems and Applications
- Architectural and Logic synthesis
- Design of Low Power Systems and Power analysis
- Packaging
- Design verification and Formal Methods
- Mixed-signal and RF design
- IC physical design automation
- Test Generation, Simulation and Diagnosis
- Design For Test
- iDDQ and iDDT testing
- Defect-based test
- Fault modeling
- Test issues in nanotechnology
- Built-In Self Test (BIST)
- Design for manufacturability (DFM)
- Memory and FPGA test and repair
- Automatic test equipment
- Analog and mixed-signal test
- On-line testing
- Test resource partitioning
- Failure analysis
- Fault tolerance
- Economics of test
- Embedded systems
- Real-time systems
- Applications Design: Media, Signal Processing, Wireless Communication and Networking, Autom Military, Secure Embedded Implementations, etc

### PAPERS SUBMISSION

To present their work at the workshop, authors are invited to submit a full paper limited to six (6) pages in the standard IEEE conference double-column format, including figures and references. Each submission should include: title, full name and affiliation of all authors, an abstract of 150 words, and keywords. It should also identify a contact author and include a complete correspondence address, phone number, fax number, and E-mail address. All submissions must be made electronically in PDF format through the IDT website. Proposals for panels, hot topic sessions and embedded tutorials are also invited.

Please ensure that your PDF file is readable by Acrobat Reader. The submission of a paper, a hot topic session or a panel proposal will be considered evidence that upon acceptance, the author(s) will present the paper or organize the panel at the workshop.

### IMPORTANT DATES

**Submission Deadline:** ~~25th September 2008~~. The deadline is extended to **9<sup>th</sup> October 2008**

**Notification of Acceptance:** **24<sup>th</sup> October 2008**

**Deadline for Paper Inclusion in Workshop Digest:** **21<sup>st</sup> November 2008**

A selection of best papers will be included in:

- 1- a special edition of the **Analog Integrated Circuits and Signal Processing**; the International Journal Springer US,
- 2- a normal edition of the **IEEE Design & Test of Computers** (the best three papers).

IDT 2008 is sponsored by the IEEE Computer Society Test Technology Technical Council (TTTC) and technically co-sponsored by the IEEE Circuits & Systems Society. More information about IDT 2008 can be found at:

<http://www.enis.rnu.tn/tttc-idt>

For general information



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